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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/813,419 | 03/30/2004 | Deepak Sabharwal | 1263-0025US | 5636 |

32375 7590 11/28/2005

SHREEN K. DANAMRAJ
DANAMRAJ & YOUST, P.C.
PREMIER PLACE, STE. 1450
DALLAS, TX 75206

| EXAMINER | |
|---|---|
| NGUYEN, DANG T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/813,419 | SABHARWAL ET AL. | |
| | Examiner | Art Unit | |
| | Dang T. Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-36* is/are pending in the application.

4a) Of the above claim(s) *1-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14,16-24,26-32 and 34-36* is/are rejected.

7)☒ Claim(s) *15,25 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

## DETAILED ACTION

1. This action is responsive to the following communications: the Application and the Information Disclosure Statement filed on March 30, 2004.

2. Claims 1 – 36 are pending in this case. Claims 1, 9, 19, and 29 are independent claims.

### *Information Disclosure Statement*

3. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed on 03/30/04 has been considered.

### *Election/Restrictions*

4. This application contains claims directed to the following patentably distinct species of the claimed invention:

Group 1, claims 1 – 8 are drawn to a Static Random Access Memory (SRAM) cell, comprising: a pair of cross-coupled inverters and a pair of access devices, and drawn to Fig. 1.

Group 2, claims 9 – 36 are drawn to a Static Random Access Memory (SRAM) instance, comprising: a plurality of SRAM cells, a row decoder, and a multiplexer, and drawn to Fig. 3.

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

During a telephone conversation with Shreen Danamraj on Thursday Nov. 10, 2005 a provisional election was made with traverse to prosecute the invention of Group II claims 9 - 36. Affirmation of this election must be made by applicant in replying to this Office action. Claims 1 – 8 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**Claims 9 - 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhavnagarwala, Patent No. US 6,515,893 B1 - filed (03/28/01) in view of Farrell et al., Pub. No. US 2003/0081492 A1, filed (10/26/01).**

**Regarding independent claim 9**, Fig. 3 of Bhavnagarwala discloses a Static Random Access Memory (SRAM) instance, comprising:

A plurality of SRAM cells organized in an array having rows and columns (Col. 1 line 32), each SRAM cell including a pair of cross-coupled inverters [306 and 302] that are coupled to form a pair of data nodes [314 and 316], wherein pull-down devices of said SRAM cells [302] forming a row are coupled together to be biased by a bias potential in standby mode ([SL] by control line 322);

However, Bhavnagarwala fails to disclose a row decoder and a multiplexer.

Fig. 2 of Farrell discloses a row decoder [130] for selectively activating wordlines based on a decoded address [A0 – A12], wherein each wordline is operable to drive a corresponding row of said array [116 and 118] (Page 2, paragraph [0017]); and a multiplexer [124 and 126] disposed between said row decoder [130] and said array [116 and 118] for deactivating said bias potential provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith (see Fig. 2).

It would have been obvious to incorporate the structure of a row decoder and multiplexer as disclosed in Farrell into the SRAM cells as disclosed in Bhavnagarwala. One having the ordinary skill in the art would have been motivated to

do this for the purpose of providing selection between memory cell for each memory arrays and memory cell within selected memory array.

**Regarding dependent claim 10**, Bhavnagarwala discloses wherein said decoded address comprises a row address. *The knowledge of using decoded address as either row address or column address is conventional and /or already well known in this art.*

**Regarding dependent claim 11**, Fig. 3 of Bhavnagarwala discloses wherein said pull-down devices [302] of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices (Col. 3 lines 15-17).

**Regarding dependent claim 12**, Bhavnagarwala discloses the claimed invention (Col. 3 lines 25-28) except for the bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts. It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply optimum range of voltage potential, since it has been held that where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

**Regarding dependent claim 13**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is operable to preserve stability of logic levels stored at said data nodes [314 and 316] of an SRAM cell [300].

**Regarding dependent claim 16**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing a body well potential (the bias potential which apply to [WL]) of said pull-down device [302].

**Regarding dependent claim 17**, Bhavnagarwala discloses wherein said bias potential is selected to preserve stability of said SRAM cells (Col. 1 lines 42-43).

**Regarding dependent claim 18**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing said pull-down devices [302] respective source terminals (Col. 3 lines 37-38).

**Regarding independent claim 19**, Fig. 3 of Bhavnagarwala discloses memory compiler for compiling at least one Static Random Access Memory (SRAM) memory instance, comprising:

a code portion for generating a plurality of SRAM memory cells organized an array having rows and columns (Col. 1 line 32), each SRAM cell including a pair of cross-coupled inverters [306 and 302] that are coupled to form a pair of data nodes [314 and 316], wherein pull-down devices of said SRAM cells forming a row are coupled together to be biased by a bias potential standby mode ([SL] by control line 322);

However, Bhavnagarwala fails to disclose a code portion for generating a plurality of SRAM memory cells, a row decoder, and a multiplexer.

Fig. 2 of Farrell discloses a code portion [112a] for generating array; a code portion [112a] for generating a row decoder [130] for selectively activating wordlines based on a decoded address [A0 – A12], wherein each wordline is operable to drive a corresponding row of said array [116 and 118] (Page 2, paragraph [0017]); and a code portion [112a] for generating a multiplexer [124 and 126] disposed between said row decoder [130] and said array [116 and 118] for deactivating said bias potential

provided to said SRAM cells of a particular row when said particular row is driven by a wordline associated therewith (see Fig. 2).

It would have been obvious to incorporate the structure of a row decoder and multiplexer as disclosed in Farrell into the SRAM cells as disclosed in Bhavnagarwala. One having the ordinary skill in the art would have been motivated to do this for the purpose of providing selection between memory cell for each memory arrays and memory cell within selected memory array.

**Regarding dependent claim 20**, Bhavnagarwala as applied to claim 19 above disclosed every aspect of applicant's claimed invention except decoded address comprises a row address.

Farrell discloses decoded address comprises a row address (Page 1, paragraph [0004] lines 16-18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated decoded address comprises a row address taught by Farrell into Bhavnagarwala's SRAM cell for the purpose of refreshing the memory cells.

**Regarding dependent claim 21**, Fig. 3 of Bhavnagarwala discloses wherein said pull-down devices [302] of said SRAM cells comprise N-channel field-effect transistor (N-FET) devices (Col. 3 lines 15-17).

**Regarding dependent claim 22**, Bhavnagarwala discloses the claimed invention (Col. 3 lines 25-28) except for the bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts. It would have been obvious to one

having ordinary skill in the art at the time the invention was made to apply optimum range of voltage potential, since it has been held that where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

**Regarding dependent claim 23**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is operable to preserve stability of logic levels stored at said data nodes [314 and 316] of an SRAM cell ([300] Col. 1 lines 42-43).

**Regarding dependent claim 26**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing a body well potential (the bias potential which apply to [WL]) of said pull-down device [302].

**Regarding dependent claim 27**, Bhavnagarwala discloses wherein said bias potential is selected to preserve stability of said SRAM cells (Col. 1 lines 42-43).

**Regarding dependent claim 28**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing said pull-down devices [302] respective source terminals (Col. 3 lines 37-38).

**Regarding independent claim 29**, Fig. 3 of Bhavnagarwala discloses a memory operation method associated with a Static Random Access Memory (SRAM) instance, said SRAM instance having a plurality of SRAM memory cells organized in an array having rows and columns (Col. 1 line 32), each SRAM cell including a pair of cross-coupled inverters [306 and 302] that are coupled to form a pair of data nodes [314 and 316], comprising:

in standby mode [SL], providing a bias potential to pull-down devices [302] of said SRAM cells that form a row of said array;

selectively activating a wordline [WL] based on a decoded address for a memory read operation; said wordline for accessing a bitcell on a row of SRAM cells (Col. 4 liines 60-65); and responsive to activating said wordline, deactivating said bias potential from said pull-down devices [302] of said row of SRAM cells [300] (Col. 5 lines 5 – 10 *mention that during read access, in which a row or wordline address/decoded must be well-known, the source line having the bias potential is maintained. Therefore, it would have been to one skill in the art that the bias potential from the source line must be down or deactivate after the read access operation).*

**Regarding dependent claim 30**, Bhavnagarwala discloses wherein said decoded address comprises a row address. *The knowledge of using decoded address as either row address or column address is conventional and /or already well known in this art.*

**Regarding dependent claim 31**, Fig. 3 of Bhavnagarwala discloses as applied to claim 29 above disclosed every aspect of applicant's claimed invention except selecting a particular bitline column based on a column address; and reading a data value stored at a select bitcell selected by said row address and said column address while continuing to activate said bias potential of remaining bitcells of said particular bitline column.

Farrell discloses selecting a particular bitline column based on a column address [A0-A12]; and and reading a data value stored at a select bitcell selected by said row

address and said column address (Page 1, paragraph [0004] lines 15-16) while continuing to activate said bias potential of remaining bitcells of said particular bitline column (Page 1, paragraph [0004]) (*be able to read and write in the memory cell, each row and column has to be selected bias potential to each memory cell*).

It would have been obvious to incorporate selecting a particular bitline and reading data value as disclosed in Farrell into the SRAM cells as disclosed in Bhavnagarwala. One having the ordinary skill in the art would have been motivated to do this for the purpose of sequentially accessing columns of memory cells.

**Regarding dependent claim 32**, Bhavnagarwala discloses the claimed invention (Col. 3 lines 25-28) except for the bias potential is approximately in a range of from about 100 millivolts to about 300 millivolts. It would have been obvious to one having ordinary skill in the art at the time the invention was made to apply optimum range of voltage potential, since it has been held that where the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

**Regarding dependent claim 34**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing a body well potential (the bias potential which apply to [WL]) of said pull-down device [302].

**Regarding dependent claim 35**, Bhavnagarwala discloses wherein said bias potential is selected to preserve stability of said SRAM cells (Col. 1 lines 42-43).

**Regarding dependent claim 36**, Fig. 3 of Bhavnagarwala discloses wherein said bias potential [PL] is applied by biasing said pull-down devices [302] respective source terminals (Col. 3 lines 37-38).

**6. Claims 14 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhavnagarwala, Patent No. US 6,515,893 B1 - filed (03/28/01) in view of Farrell et al., Pub. No. US 2003/0081492 A1, filed (10/26/01) and further view of Chow et al., Patent No.: US 6,920,060 B2 – filed (8/14/02).**

**Regarding dependent claims 14 and 24**, Bhavnagarwala and Ferrell as applied to claims 9 and 19 above disclosed every aspect of applicant's claimed invention except for the multiplexer comprises a plurality of bias switch elements, each corresponding to a wordline.

Figs. 4 and 5A of Chow disclose a multiplexer [54] comprises a plurality of bias switch elements [1,2,3], each corresponding to a wordline [48].

Bhavnagarwala/Ferrell and Chow are common subject matter for switch elements. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporated Chow's bias switch into Ferrell's multiplexer for the purpose of selecting a particular row one at a time.

***Allowable Subject Matter***

7. Claims 15, 25, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

**With respect to claims 15 and 25**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "each bias switch element comprises logic circuitry driven by a corresponding wordline to deactivate said bias potential when said corresponding wordline is driven high".

**With respect to claim 33**, the primary reason for indication of allowable subject matter is that the prior art fails to teach or suggest "upon completion said reading, re-activating said bias potential to said row of SRAM cells associated with said row address".

***Prior art***

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Houston Pub. No. US 2005/0128789 A1 Pub. Date: Jun. 16, 2005

Chappell et al. Pub. No. : US 2003/0012048 A1 Pub. Date: Jan. 16, 2003

***Contact Information***

9. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's

supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 11/17/2005

VAN THU NGUYEN
PRIMARY EXAMINER